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(54) Semiconductor device substrate and method of manufacturing the same

(57) A semiconductor device is provided that includes a substrate (1) having a first side, a second side and a through-hole (4). An external connection terminal (3) is located on the first side of the substrate (1), and a chip connection terminal (2) is located on the second side of the substrate. The chip connection terminal (2) is electrically connected to the external connection terminal (3) via the through-hole (4). The external connection terminal (3), the inner portion of the through-hole (4) and a first portion of the chip connection terminal (2) have a hard gold plating, and a second portion of the chip connection terminal (2) has a soft gold plating.

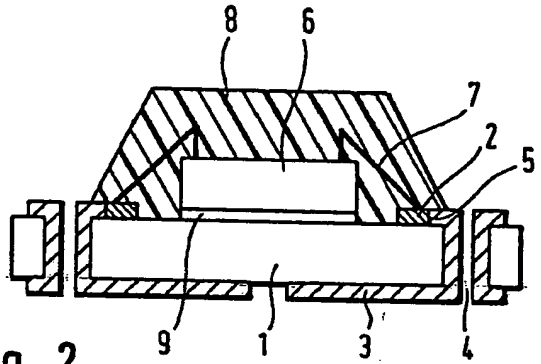


Fig. 2

EP 0 810 656 A2

Description

FIELD OF THE INVENTION

The present invention relates to a semiconductor device substrate, and more specifically to a semiconductor device substrate for use in a semiconductor device of the type used in card-type modules, information memory devices, IC cards, or the like, and a method of manufacturing the same.

BACKGROUND OF THE INVENTION

Recently, card-type memory devices such as IC cards have been brought into practical use. In a card-type memory device, a semiconductor chip is mounted in a semiconductor package. Typically, the semiconductor package has the chip resin-molded on one side and a planar-type external connection terminal on the other side. The chip may be a nonvolatile semiconductor memory device or any other type of semiconductor chip.

Figures 9, 10(a), and 10(b) show a conventional semiconductor package for a card-type memory device. Figure 9 is a cross-sectional view of the semiconductor package, Figure 10(a) is a perspective view of the chip side of the semiconductor package, and Figure 10(b) is a perspective view of the external terminal side of the semiconductor package. As shown in Figure 9, a substrate 1 is formed of resin, which has a thickness of approximately 0.1 - 0.4 mm, and a semiconductor chip 6 is bonded to the substrate 1 by an adhesive 9. A gold wire 7 provides an electrical connection between a chip connection terminal 2 of the substrate 1 and a bonding pad of tile semiconductor chip 6. The chip side of the substrate 1 is molded by a resin 8 that covers the semiconductor chip 6, and an external connection terminal 3 is provided on the other side of the substrate 1. The external connection terminal 3 is electrically connected to the chip connection terminal 2 via a through-hole 4 that penetrates the substrate 1.

Figure 8 shows a cross-sectional view of the substrate used in the conventional semiconductor package of Figure 9. (In the different figures, elements that are the same are represented by the same reference numerals and duplicate descriptions thereof are omitted.) The chip connection terminal 2, which is located on the chip side of the substrate 1, is typically plated with soft gold with a purity of 99.9% or higher. The soft gold on the chip connection terminal 2 provides a good connection between the bonding wire 7 and the chip connection terminal 2 because soft gold or aluminum is typically used for the bonding wire that is connected between the chip's bonding pad and the chip connection terminal of the substrate 1. On the other hand, the external connection terminal 3, which is located on the side of the substrate opposite the semiconductor chip 6, is typically plated with hard gold with a purity of approximately 99%. Hard gold is used for the external connection terminal because it offers a greater resistance to damage. Thus, a boundary 5 between the soft gold plating and the hard gold plating is located at a central portion of the through-hole 4. For simplification, Figure 8 does not individually show the gold plating, nickel plating, and copper plating and foil that are described below. These layers are collectively shown as the chip connection terminal and the external connection terminal in Figure 8.

Figures 11(a) through 11(f) show a typical manufacturing process for the conventional semiconductor device substrate described above. First, copper foils 24 with an illustrative thickness of about 18 μm are attached using an adhesive to both sides of a resin substrate 1, as shown in Figure 11(a). The substrate 1 is then drilled to open a through-hole 4, as shown in Figure 11(b). Next, as shown in Figure 11(c), the entire substrate is plated with copper so that copper plating 25 is provided on the inner side of the through-hole and on both sides of the substrate. Thus, the copper plating provides an electrical connection between the two sides of the substrate. A photoresist-type dry film is then pasted onto the copper of the substrate and a copper interconnection is formed through exposure of light, patterning, and etching of the copper, as shown in Figure 11(d).

The copper interconnections are typically formed of both copper foils and copper plating because the copper foils can be used to easily and quickly increase the thickness of the connection by merely pasting them onto the substrate. However, the copper foil cannot be attached to the inner side of the through-hole to complete the interconnection. On the other hand, it is rather difficult to increase the thickness of the connection terminal through copper plating because of the slow progress of the plating process. In cases where a low relative thickness or slow progress are not drawbacks, it is possible to omit the copper foils and use only the copper plating to form the copper interconnections.

In the next step of the manufacturing process, the chip-mounting side of the substrate is entirely masked using a tape or photoresist-type dry film. Bright nickel (not shown) and hard gold are then consecutively plated on the substrate to provide a hard gold plating 3 over the copper interconnection on the external terminal side of the substrate and on the inside of the through-hole 4, as shown in Figure 11(e). Then, the hard gold-plated external terminal side of the substrate is entirely masked using a tape or dry film. Non-bright or semi-bright nickel (not shown) and soft gold are then consecutively plated on the substrate to provide soft gold plating 2 over the copper interconnection on the chip-mounting side of the substrate and on the inside of the through-hole 4, as shown in Figure 11(f). The nickel plating is interposed between the copper plating and the gold plating because the intervening nickel layer prevents a slow diffusion of the gold into the copper. In another typical manufacturing process, the order of the gold plating is reversed so that soft gold is first plated on the chip-mounting side and then hard gold is plated on the exter-

nal terminal side of the substrate.

In such conventional manufacturing processes, one side of the through-hole 4 is closed by the masking during both soil gold and hard gold plating. As a result, air builds up in the through-hole 4 and the plating solution is prevented from flowing through the through-hole 4. Therefore, in some cases, no plating is attained at the central portion of the through-hole 4. Whenever the through-hole 4 has portions that are not plated by either the soil gold or hard gold, the underlying metal layer of copper or nickel is exposed to oxygen and the like. This allows corrosive action to occur in the exposed portion of the through-hole so that a breakage of the interconnection between the two sides of the substrate may result.

SUMMARY OF THE INVENTION

In view of these problems, it is an object of the present invention to remove the above-mentioned drawbacks and to provide a semiconductor substrate in which the inside of the through-hole is completely plated in order to improve the reliability of the interconnection. To achieve this object, the through-hole in the substrate is not blocked when it is selectively plated. As a result, the plating solution readily flows through and near the through-hole so that plating is provided on the surface of the through-hole. Thug, there is no plating boundary located within the through-hole, so corrosive action is prevented in the underlying layers in the through-hole portion and the reliability of the interconnection that passes through the through-hole is improved. The present invention also provides a method of manufacturing such a device.

According to a first embodiment of the present invention, a semiconductor device is provided that includes a substrate having a first side, a second side, and a through-hole. An external connection terminal is located on the first side of the substrate, and a chip connection terminal is located on the second side of the substrate. The chip connection terminal is electrically connected to the external connection terminal via the through-hole. The external connection terminal, the inner portion of the through hole, and a first portion of the chip connection terminal have a hard gold plating, and a second portion of the chip connection terminal has a soft gold plating.

According to a second embodiment of the present invention, a semiconductor device is provided that includes a substrate having a first side, a second side, and a through-hole. An external connection terminal is located on the first side of the substrate, and a chip connection terminal is located on the second side of the substrate. The chip connection terminal is electrically connected to the external connection terminal via the through-hole. The chip connection terminal, the inner portion of the through hole, and a first portion of the external connection terminal have a soft plating, and a second portion of the external connection terminal has a hard gold plating.

According to a third embodiment of the present invention, a method is provided for manufacturing a semiconductor device by making an interconnection pattern of copper plating on a first side and a second side of a substrate and on the inner side of a through-hole. A first mask is formed on the first side of the substrate so as to cover a portion of the interconnection pattern on the first side without covering the through-hole. Nickel and then hard gold are plated on the portion of the interconnection pattern that is not covered by the first mask (including the inner side of the through-hole), and then the first mask is removed. A second mask is then formed to cover the portion of the interconnection pattern that was plated with hard gold. Nickel and then soft gold are plated on the portion of the interconnection pattern that is not covered by the second mask, and then the second mask is removed.

According to a fourth embodiment of the present invention, a method is provided for manufacturing a semiconductor device by making an interconnection pattern of copper plating on a first side and a second side of a substrate and on the inner side of a through-hole. A first mask is formed on the first side of the substrate so as to cover a portion of the interconnection pattern on the first side and the through-hole. Nickel and then soft gold are plated on the portion of the interconnection pattern that is not covered by the first mask, and then the first mask is removed. A second mask is then formed to cover the portion of the interconnection pattern that was plated with soft gold. Nickel and then hard gold are plated on the portion of the interconnection pattern that is not covered by the second mask (including the inner side of the through-hole), and then the second mask is removed.

According to a fifth embodiment of the present invention, a semiconductor device is provided that includes a substrate having a first side, a second side, and a through-hole. An external connection terminal is located on the first side of the substrate, and a chip connection terminal is located on the second side of the substrate. The chip connection terminal is electrically connected to the external connection terminal via the through-hole. A semiconductor chip is attached to the second side of the substrate and electrically connected to the chip connection terminal, and a resin molding covers at least a portion of the second side of the substrate. The external connection terminal, the inner portion of the through hole, and a first portion of the chip connection terminal have a hard gold plating, and a second portion of the chip connection terminal has a soft gold plating.

According to a sixth embodiment of the present invention, a semiconductor device is provided that includes a substrate having a first side, a second side, and a through-hole. An external connection terminal is located on the first side of the substrate, and a chip connection terminal is located on the second side of the substrate. The chip connection terminal is electrically

connected to the external connection terminal via the through-hole. A semiconductor chip is attached to the second side of the substrate and electrically connected to the chip connection terminal, and a resin molding covers at least a portion of the second side of the substrate. The chip connection terminal, the inner portion of the through hole, and a first portion of the external connection terminal have a soft plating, and a second portion of the external connection terminal has a hard gold plating.

The some embodiments of the present invention provide a card-type module that includes the semiconductor device of the previously-described embodiments. Additionally, some embodiments of the present invention provide a memory device having such a card-type module and a main body. The main body includes a first connector connected to the external connection terminal of the card-type module, a second connector connected to an apparatus, and an interface control circuit connected to the first and second connectors.

Other objects, features, and advantages of the present invention will become apparent from the following detailed description. It should be understood, however, that the detailed description and specific examples, while indicating preferred embodiments of the present invention, are given by way of illustration only and various modifications may naturally be performed without deviating from the scope of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view showing a substrate according to a preferred embodiment of the present invention;

Figure 2 is a cross-sectional view showing a semiconductor device according to a preferred embodiment of the present invention;

Figure 3 is a cross-sectional view showing another embodiment of a semiconductor device according to the present invention;

Figure 4 is a top view showing the substrate according to the preferred embodiment of the present invention;

Figure 5 is a perspective view showing a card-type module according to a preferred embodiment of the present invention;

Figures 6(a) through 6(f) are views showing a manufacturing process for the substrate according to the preferred embodiment of the present invention;

Figures 7(a) and 7(b) are perspective views showing an adapter card according to a preferred embodiment of the present invention;

Figure 8 is a cross-sectional view showing a conventional substrate;

Figure 9 is a cross-sectional view showing a conventional semiconductor device;

Figures 10(a) and 10(b) are perspective views showing the conventional semiconductor device; and

Figures 11(a) through 11(f) are views showing a process for manufacturing the substrate of the conventional semiconductor device.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described in detail hereinbelow with reference to the attached drawings.

Figure 1 shows a semiconductor device substrate according to a preferred embodiment of the present invention, and Figure 6 shows a preferred manufacturing process for the semiconductor device substrate of Figure 1. First, copper foils 24 with an illustrative thickness of 18 μm are attached using an adhesive to both sides of a resin substrate 1, as shown in Figure 6(a). In the preferred embodiment, the substrate is a high strength substrate formed of a glass fiber framework that is covered by an epoxy resin. A through-hole 4 is then formed by drilling through the substrate, as shown in Figure 6(b). Next, as shown in Figure 6(c), the entire substrate is plated with copper so that copper plating 25 is provided on the inner side of the through-hole 4 and on both sides of the substrate 1. The copper plating 25, which provides an electrical connection between the two sides of the substrate, is illustratively formed with a thickness of about 10 to 15 μm. As shown in Figure 6(d), a copper interconnection is then formed using a photoresist-type dry film or the like. For example, when a dry film is used, it is pasted onto the copper 25 of the substrate and a copper interconnection is formed by sequentially performing exposure to light, patterning, and etching of the copper.

Next, the portion of the interconnection on the chip-mounting side of the substrate is masked. However, while the chip connection terminal is masked, the through-hole 4 is not masked. Such a mask can be formed by adhering a pre-shaped tape to the substrate, or by applying a dry film over the entire chip-mounting side of the substrate and then patterning the film using a lithography technique or the like. The substrate is then consecutively subjected to bright-nickel plating (not shown) and hard gold plating to provide a hard gold plating 3 over the interconnection pattern, as shown in Figure 6(e). Because the through-hole 4 is not closed at its top or bottom by the mask, the plating solution readily flows through and near the through-hole 4. Thus, the hard gold plating 3 covers the entire copper interconnection on the external terminal side of the substrate, the entire copper interconnection layer on the inner side of the through-hole 4, and the unmasked portion of the copper interconnection on the chip-mounting side of the substrate.

After removing the above-mentioned mask, the hard gold-plated portion 3 is newly masked in the same manner as described above. Then, the unmasked portion is consecutively subjected to non-bright nickel plat-

ing (not shown) and soft gold plating to provide a soft gold plating 2 over the interconnection pattern. The new mask is then also removed. As a result, the soft-gold plating 2 is provided on the unmasked portion of the chip connection terminal (of the copper interconnection) on the chip-mounting side of the substrate, as shown in Figure 6(f). For simplification, Figures 1-3 do not individually show the gold plating, nickel plating, and copper plating and foil described above. These layers are collectively shown as the chip connection terminal and the external connection terminal in these figures.

Accordingly, in the embodiment of the present invention described above, the entire copper interconnection layer on the inner side of the through-hole 4 is covered with the hard gold plating 3 so that the boundary 5 between the soft gold plating and the hard gold plating is located outside of the through-hole 4.

In further embodiments of the present invention, the above gold plating order is reversed. That is, soft gold is first plated to the chip connection terminal on the chip-mounting side of the substrate, and then hard gold is plated on the entire copper interconnection on the external terminal side of the substrate, the entire copper interconnection layer on the inner side of the through-hole 4, and the non-soft gold plated portion of the copper interconnection on the chip-mounting side of the substrate.

Figure 4 shows a top view of the semiconductor device substrate of Figure 1. An interconnection 12 extends from a chip connection terminal 11, through a through-hole 4, and to an external connection terminal on the opposite side of the substrate 1. A semiconductor chip is mounted on a chip mount surface portion 13 of the substrate, and resin molding is performed on the area within resin molding boundary line 14. Further, a cutting line 15 shows the line along which the semiconductor module is cut after the substrate 1 is mounted with a semiconductor chip and then resin molded. A gold plating boundary line 16 represents a boundary between the soft gold plating and the hard gold plating of the interconnections. More specifically, the inner side of the gold plating boundary line 16 is plated with soft gold, and the outer side is plated with hard gold. In further embodiments, the gold plating boundary line 16 is on the outer side of the resin molding boundary line 14.

Figure 2 shows a semiconductor package according to a preferred embodiment of the present invention. The semiconductor package is formed by bonding a semiconductor chip 6 to the substrate of Figure 1 by an adhesive 9. A bonding pad of the semiconductor chip 6 is connected by a gold wire 7 to the chip connection terminal of the substrate 1, and the chip-mounting side of the substrate is molded by resin 8. In the preferred embodiment, the resin 8 is an epoxy resin and the semiconductor chip is a nonvolatile semiconductor memory device such as a NAND-type Flash EEPROM. However, the chip may be any type of semiconductor chip. Additionally, in another embodiment of the semiconductor package of the present invention, the semiconductor chip is connected to the chip connection terminal of the substrate through a flip-chip-type connection that utilizes a bump 10, as shown in Figure 3.

The semiconductor packages of Figures 2 and 3 may be used in a card-type module, as shown in Figure 5. The card-type module is smaller than a typical IC card, which is connected to a personal computer or the like. For example, in the preferred embodiment, the card-type module employs a base card 18 that is illustratively formed of resin and has an illustrative length, width, and thickness of 37 mm by 45 mm by 0.76 mm. The base card is provided with a recessed portion 18a that holds the semiconductor package. More specifically, the semiconductor package 17 is bonded to the base card 18 by burying the resin-molded side of the semiconductor package 17 into the recessed portion 18a of the base card in such a manner that the external terminal 3 side of the package is flush with the surface of the base card 18. In the preferred embodiment, the card-type module contains a nonvolatile semiconductor memory device so that it is analogous to a floppy disk. That is, the card-type module contains the storage portion but not the driver portion of the complete storage device. The driver portion (i.e., processing circuitry and the like) is located in an adaptor card (of a personal computer), a digital camera, or other electronic device. Thus, the storage portion of the memory device can be exchanged, just like a floppy disk, by exchanging the card-type module.

Figures 7(a) and 7(b) show an adapter card that allows the card-type module of Figure 5 to be connected to a PCMCIA card slot or the like so that the card-type module can be interfaced with a personal computer, digital camera, or other electronic device. As shown in Figure 7(a), the adapter card 20 has the outer appearance of a PCMCIA card and includes an insertion hole 20a for receiving a card-type module 19. As shown in Figure 7(b), one connector 23 allows the adaptor card to be attached to the PCMCIA card slot of a personal computer, electronic device, or the like, and another connector 22 in the interior of the adapter card 20 contacts with the external connection terminals 3 of the card-type module 19. Additionally, an interface circuit 21 functions as an interface between the card-type module 19 and an external apparatus, such as a personal computer.

In alternative embodiments, the adapter is of a form other than the card-type that is attached to a PCMCIA card slot. In still other embodiments, a drive circuit or the like may be provided in the interior of the adapter card 20 to control the card-type module. Furthermore, the connector 22 that contacts with the external connection terminals 3 of the card-type module may be provided, typically along with the interface circuit 21 and the like, in the main body of a personal computer, digital camera, or other electronic device.

While in the embodiments described above the substrate is formed of resin, in further embodiments, the substrate is formed of TAB tape. More specifically, tape automating bonding ("TAB") is used to form a thinner

semiconductor package in which the wires connected to the chip electrodes are formed by copper plating on the insulation tape film. Further, in the embodiments described above, the semiconductor substrate has hard gold plating located on the external terminal side of the substrate, the inner side of the through-hole, and a portion of the chip-mounting side of the substrate. However, the present invention is not limited to only that specific structure. For example, the sides could be reversed, the soft gold and hard gold plating portions could be switched, or all soft gold plating could be used.

As described above, the present invention provides a semiconductor substrate having a through-hole which is not blocked when it is selectively plated. As a result, the plating solution readily flows through and near the through-hole so that plating is provided on the surface of the through-hole. Furthermore, there is no plating boundary located within the through-hole, so corrosive action is prevented in the underlying layers in the through-hole portion. Thus, the reliability of the interconnection that passes through the through-hole is improved.

While there has been illustrated and described what are presently considered to be the preferred embodiments of the present invention, it will be understood by those in the art that various other modifications may be made, and equivalents may be substituted, without departing from the true scope of the invention. Additionally, many modifications may be made to adapt a particular situation to the teachings of the present invention without departing from the central inventive concept described herein. Therefore, it is intended that the present invention not be limited to the particular embodiments disclosed, but that the invention include all embodiments falling within the scope of the appended claims.

Claims

1. A semiconductor device comprising:

   a substrate having a first side, a second side, and a through-hole formed so as to penetrate the first side and the second side;
   an external connection terminal on the first side of the substrate; and
   a chip connection terminal on the second side of the substrate, the chip connection terminal being electrically connected to the external connection terminal via the through-hole,
   wherein the external connection terminal, the inner portion of the through hole, and a first portion of the chip connection terminal have a hard gold plating, and
   a second portion of the chip connection terminal has a soft gold plating.

2. The semiconductor device as defined in claim 1, wherein the external connection terminal has a flat portion.

3. The semiconductor device as defined in claim 1, wherein the chip connection terminal has a flat portion.

4. The semiconductor device as defined in claim 1, wherein the chip connection terminal is located on the periphery of the substrate.

5. A semiconductor device comprising:

   a substrate having a first side, a second side, and a through-hole formed so as to penetrate the first side and the second side;
   an external connection terminal on the first side of the substrate; and
   a chip connection terminal on the second side of the substrate, the chip connection terminal being electrically connected to the external connection terminal via the through-hole,
   wherein the chip connection terminal, the inner portion of the through hole, and a first portion of the external connection terminal have a soft plating, and
   a second portion of the external connection terminal has a hard gold plating.

6. The semiconductor device as defined in claim 5, wherein the external connection terminal has a flat portion.

7. The semiconductor device as defined in claim 5, wherein the chip connection terminal has a flat portion.

8. The semiconductor device as defined in claim 5, wherein the chip connection terminal is located on the periphery of the substrate.

9. A method of manufacturing a semiconductor device, said method comprising the steps of:

   making an interconnection pattern of copper plating on a first side and a second side of a substrate and on the inner side of a through-hole using a photolithography technique and an etching technique, the through-hole formed so as to penetrate the first and second sides;
   forming a first mask on the first side of the substrate so as to cover a portion of the interconnection pattern on the first side without covering the through-hole;
   plating nickel and then hard gold on the portion of the interconnection pattern that is not covered by the first mask, the plated portion including the inner side of the through-hole;
   removing the first mask;
   forming a second mask to cover the portion of

the interconnection pattern that was plated with hard gold;
plating nickel and then soft gold on the portion of the interconnection pattern that is not covered by the second mask; and
removing the second mask.

10. The method as defined in claim 9, wherein the portion of the interconnection pattern that is covered by the hard gold functions as an external connection terminal.

11. A method of manufacturing a semiconductor device, said method comprising the steps of:

making an interconnection pattern of copper plating on a first side and a second side of a substrate and on the inner side of a through-hole using a photolithography technique and an etching technique, the through-hole formed so as to penetrate the first and second sides;
forming a first mask on the first side of the substrate so as to cover a portion of the interconnection pattern on the first side and the through-hole;
plating nickel and then soft gold on the portion of the interconnection pattern that is not covered by the first mask;
removing the first mask;
forming a second mask to cover the portion of the interconnection pattern that was plated with soft gold;
plating nickel and then hard gold on the portion of the interconnection pattern that is not covered by the second mask, the plated portion including the inner side of the through-hole; and
removing the second mask.

12. The method as defined in claim 11, wherein the portion of the interconnection pattern that is covered by the hard gold functions as an external connection terminal.

13. A method of manufacturing a semiconductor device, said method comprising the steps of:

forming, on a substrate having a through-hole that penetrates from a first side to a second side of the substrate, hard gold plating on at least the periphery of the through-hole on the first side of the substrate, the periphery of the through-hole on the second side of the substrate, and the inner side of the through-hole; and
forming soft gold plating on at least a portion of the first side of the substrate that is not covered by the hard gold plating.

14. The method as defined in claim 13, wherein the portion of the substrate that is covered by the hard gold plating functions as an external connection terminal.

15. A method of manufacturing a semiconductor device, said method comprising the steps of:

forming, on a substrate having a through-hole that penetrates from a first side to a second side of the substrate, soft gold plating on at least the periphery of the through-hole on the first side of the substrate, the periphery of the through-hole on the second side of the substrate, and the inner side of the through-hole; and
forming hard gold plating on at least a portion of the first side of the substrate that is not covered by the soft gold plating.

16. The method as defined in claim 15, wherein the portion of the substrate that is covered by the hard gold plating functions as an external connection terminal.

17. A semiconductor device comprising:

a substrate having a first side, a second side, and a through-hole formed so as to penetrate the first side and the second side;
an external connection terminal on the first side of the substrate;
a chip connection terminal on the second side of the substrate, the chip connection terminal being electrically connected to the external connection terminal via the through-hole;
a semiconductor chip attached to the second side of the substrate and electrically connected to the chip connection terminal; and
a resin molding over at least a portion of the second side of the substrate,
wherein the external connection terminal, the inner portion of the through hole, and a first portion of the chip connection terminal have a hard gold plating, and
a second portion of the chip connection terminal has a soft gold plating.

18. The semiconductor device as defined in claim 17, wherein the chip connection terminal and the semiconductor chip are connected using a wire.

19. The semiconductor device as defined in claim 17, wherein the chip connection terminal and the semiconductor chip are connected using a flip-chip connection.

20. A semiconductor device substrate comprising:

a substrate having a first side, a second side, and a through-hole formed so as to penetrate the first side and the second side;
an external connection terminal on the first side of the substrate;
a chip connection terminal on the second side of the substrate, the chip connection terminal being electrically connected to the external connection terminal via the through-hole;
a semiconductor chip attached to the second side of the substrate and electrically connected to the chip connection terminal; and
a resin molding over at least a portion of the second side of the substrate,
wherein the chip connection terminal, the inner portion of the through hole, and a first portion of the external connection terminal have a soft gold plating; and
a second portion of the external connection terminal has a hard gold plating.

21. The semiconductor device as defined in claim 20, wherein the chip connection terminal and the semiconductor chip are connected using a wire.

22. The semiconductor device as defined in claim 20, wherein the chip connection terminal and the semiconductor chip are connected using a flip-chip connection.

23. A card-type supporter that includes a semiconductor device, the card-type module comprising:

a card-type supporter having a recess;
a substrate having a first side, a second side, and a through-hole formed so as to penetrate the first side and the second side;
an external connection terminal on the first side of the substrate;
a chip connection terminal on the second side of the substrate, the chip connection terminal being electrically connected to the external connection terminal via the through-hole;
a semiconductor chip attached to the second side of the substrate and electrically connected to the chip connection terminal; and
a resin molding over the at least a portion of the second side of the substrate,
wherein the external connection terminal, the inner portion of the through hole, and a first portion of the chip connection terminal have a hard gold plating,
a second portion of the chip connection terminal has a soft gold plating, and
the substrate is bonded to the recess of the card-type supporter by burying the resin-molded side of the substrate.

24. A card-type module that includes a semiconductor device, the card-type module comprising:

a card-type supporter having a recess;
a substrate having a first side, a second side, and a through-hole formed so as to penetrate the first side and the second side;
an external connection terminal on the first side of the substrate;
a chip connection terminal on the second side of the substrate, the chip connection terminal being electrically connected to the external connection terminal via the through-hole;
a semiconductor chip attached to the second side of the substrate and electrically connected to the chip connection terminal; and
a resin molding over the at least a portion of the second side of the substrate,
wherein the chip connection terminal, the inner portion of the through hole, and a first portion of the external connection terminal have a soft gold plating,
a second portion of the external connection terminal has a hard gold plating, and
the substrate is bonded to the recess of the card-type supporter by burying the resin-molded side of the substrate.

25. A memory device comprising:

a card-type module including:

a card-type supporter having a recess;
a substrate having a first side, a second side, and a through-hole formed so as to penetrate the first side and the second side;
an external connection terminal on the first side of the substrate;
a chip connection terminal on the second side of the substrate, the chip connection terminal being electrically connected to the external connection terminal via the through-hole;
a semiconductor chip attached to the second side of the substrate and electrically connected to the chip connection terminal: and
a resin molding over the at least a portion of the second side of the substrate;

and
a main body including:

a first connector connected to the external connection terminal of the card-type module;
a second connector connected to an apparatus; and
an interface control circuit connected to the

first and second connectors,

wherein the external connection terminal, the inner portion of the through hole, and a first portion of the chip connection terminal have a hard gold plating,
a second portion of the chip connection terminal has a soft gold plating, and
the substrate is bonded to the recess of the card-type supporter by burying the resin-molded side of the substrate.

26. A memory device comprising:

a card-type module including:

a card-type supporter having a recess;
a substrate having a first side, a second side, and a through-hole formed so as to
penetrate the first side and the second side;

an external connection terminal on the first side of the substrate;
a chip connection terminal on the second side of the substrate, the chip connection terminal being electrically connected to the external connection terminal via the through-hole;
a semiconductor chip attached to the second side of the substrate and electrically connected to the chip connection terminal; and
a resin molding over the at least a portion of the second side of the substrate;

and
a main body including:

a first connector connected to the external connection terminal of the card-type module;
a second connector connected to an apparatus; and
an interface control circuit connected to the first and second connectors,

wherein the chip connection terminal, the inner portion of the though hole, and a first portion of the external connection terminal have a soft gold plating,
a second portion of the external connection terminal has a hard gold plating, and
the substrate is bonded to the recess of the card-type supporter by burying the resin-molded side of the substrate.

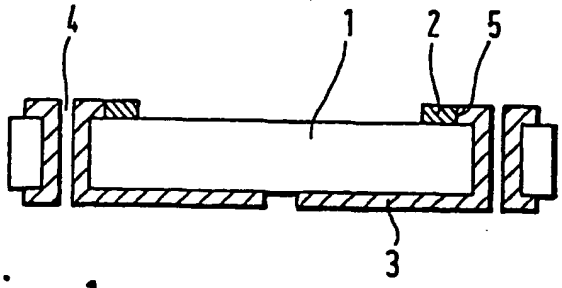


Fig. 1

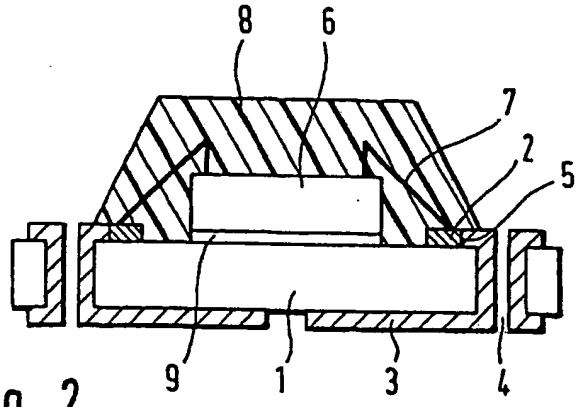


Fig. 2

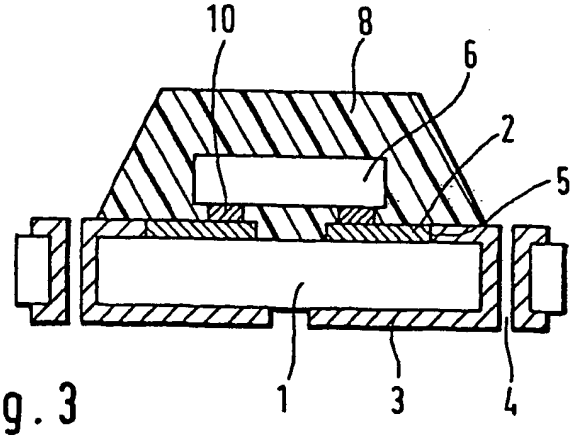


Fig. 3

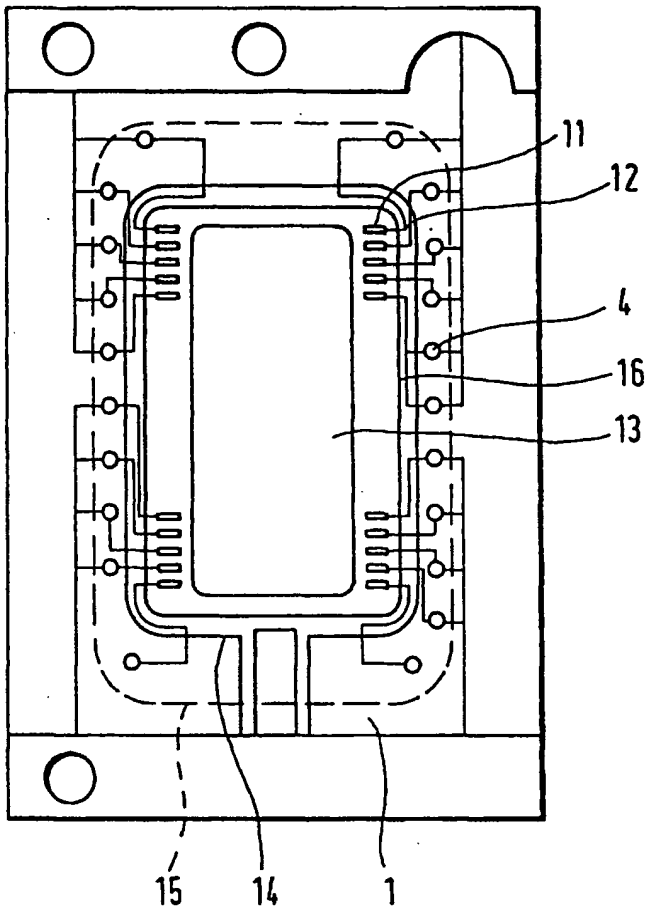


Fig. 4

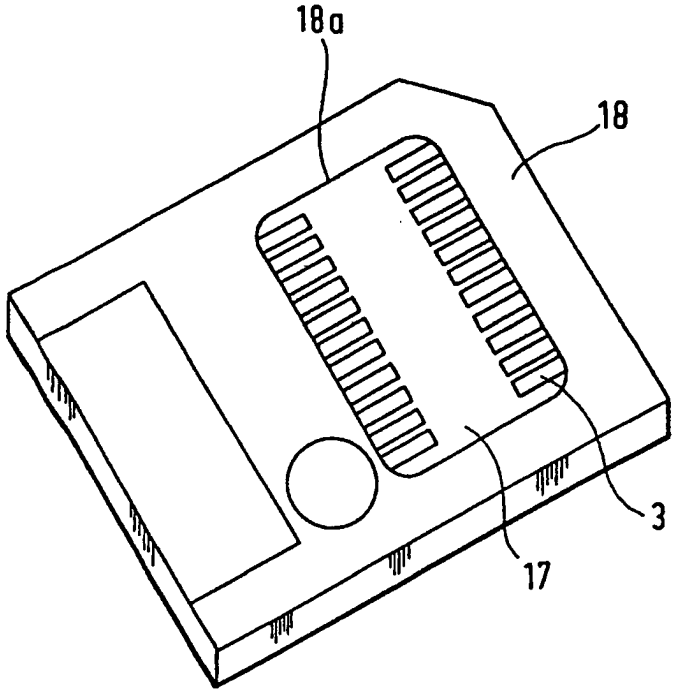


Fig. 5

Fig. 6(a)

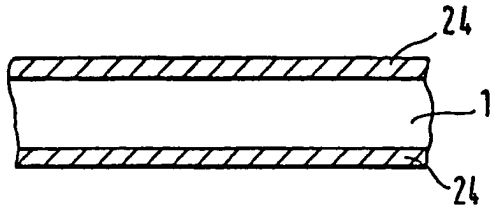


Fig. 6(b)

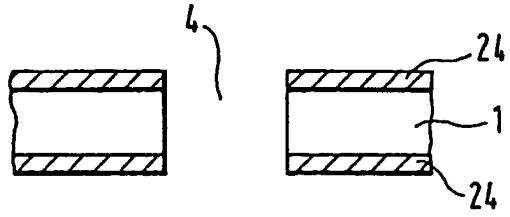


Fig. 6(c)

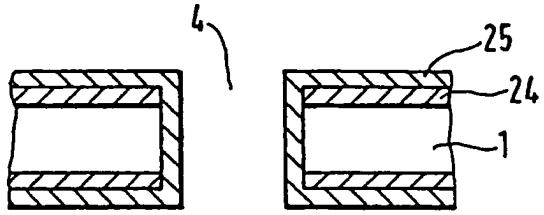


Fig. 6(d)

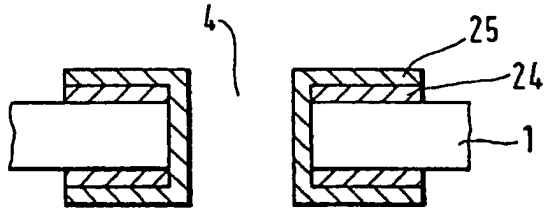


Fig. 6(e)

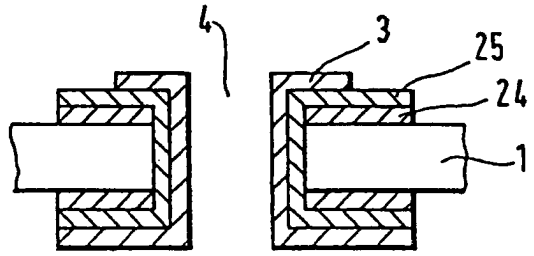
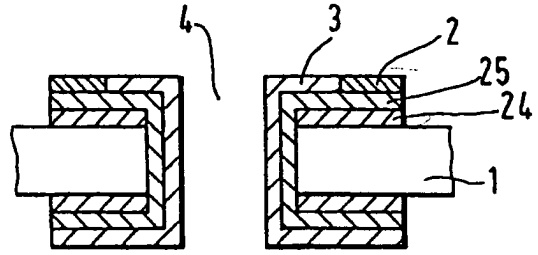


Fig. 6(f)



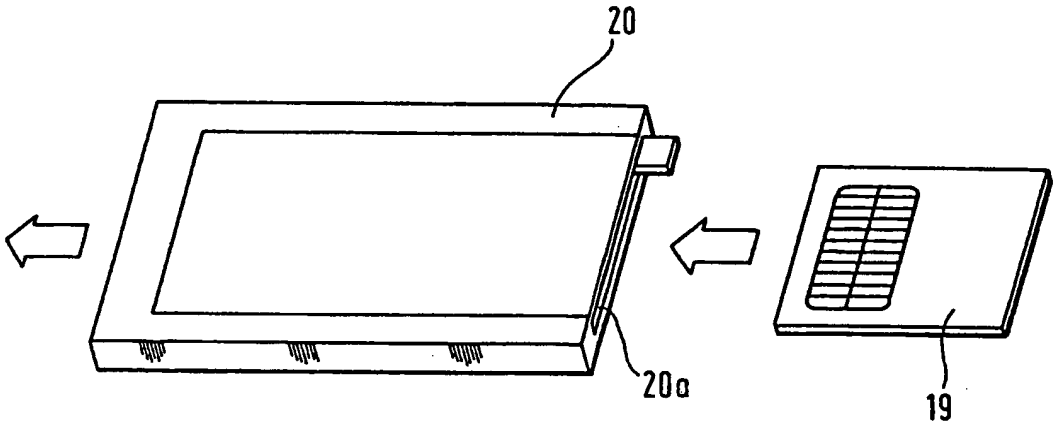


Fig. 7(a)

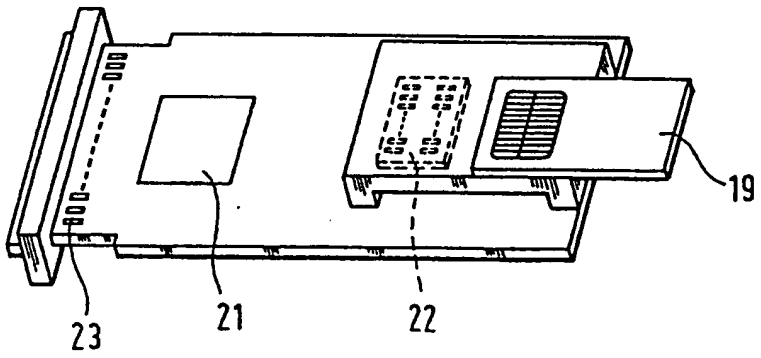


Fig. 7(b)

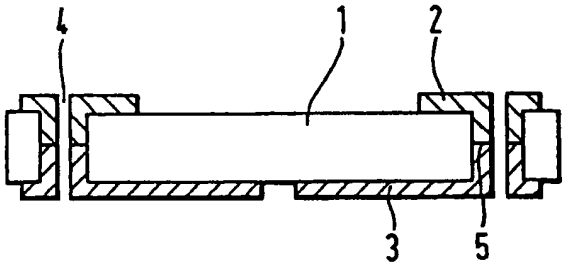


Fig.8

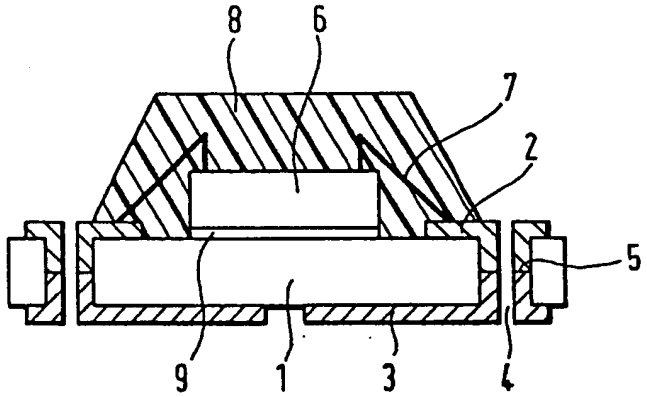


Fig.9

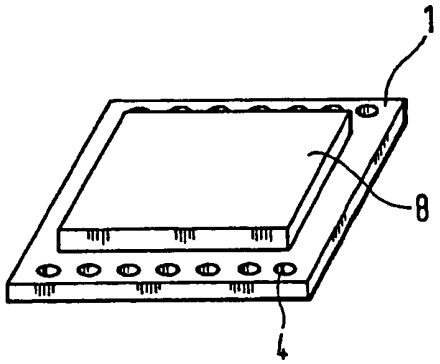


Fig.10(a)

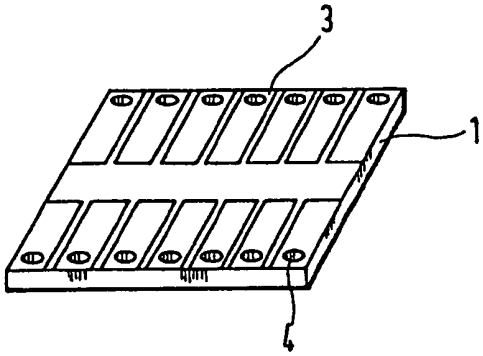


Fig.10(b)

Fig. 11(a)

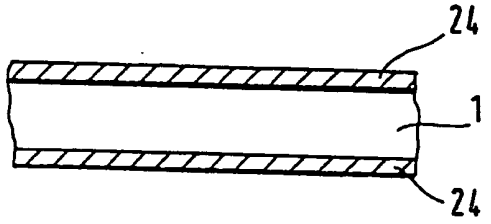


Fig. 11(b)

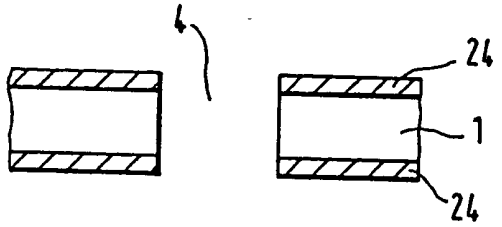


Fig. 11(c)

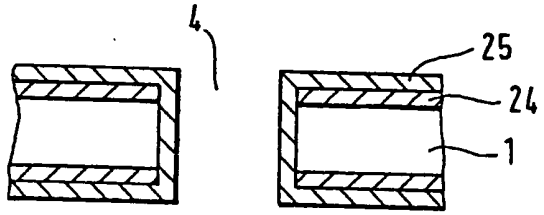


Fig. 11(d)

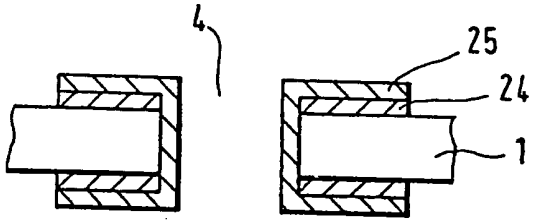


Fig. 11(e)

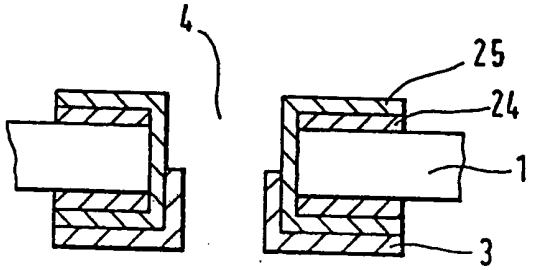


Fig. 11(f)